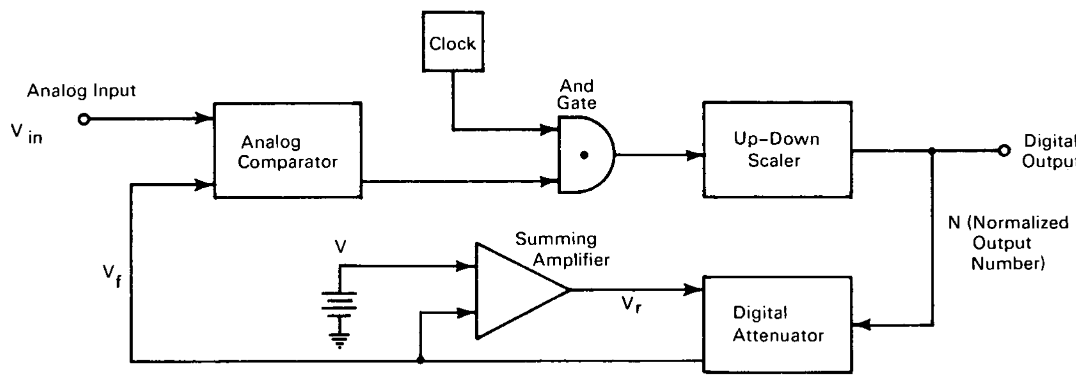
NASA TECH BRIEF

Nonlinear Feedback Reduces Analog-to-Digital Converter Error



The problem: To design a simple, accurate analog-to-digital converter, (ADC) that exhibits minimum error characteristics. The accuracy of conventional linear ADC's suffers at low operating levels due to their inherent quantization error, i.e., an inability to measure increments smaller then the least significant digit.

The solution: A nonlinear analog-to-digital converter that measures the level of an analog input and continuously adjusts the scale sensitivity of the digital readout to attain an effective increase in accuracy. As the output level decreases the scale sensitivity increases to retain a more nearly constant accuracy as expressed in percentage of reading, thus permitting the acquisition of more accurate low-level data.

How it's done: In order to obtain the nonlinearity necessary for scale adjustment, an accurate nonlinearity is placed in the conventional feedback path. This is done in the feedback elements consisting of the summing amplifier, reference voltage, and digital attenuator. These elements are capable of a high degree of accuracy as compared to other possible nonlinear elements.

A typical nonlinear analog-to-digital converter consists of six basic subsystems: an analog comparator, a clock and control gate, an up-down scaler, a digital attenuator, a summing amplifier, and a fixed voltage source.

The analog voltage to be sampled is fed into the analog comparator, which produces an output if there is any difference between V_{in} and V_f (the feedback voltage). Any output from the comparator turns the AND gate on and allows the clock signal to be fed to the up-down scaler. The up-down scaler produces the digital output in the form of an output number.

The nonlinear feedback loop consists of the digital attenuator, the summing amplifier, and the fixed voltage supply V. The feedback voltage V_f is proportional to the product of the reference voltage V_r and the normalized digital output N, where N is the ratio of the output number to the number which represents full scale. The summing amplifier adds the fixed voltage V to the feedback voltage and passes the summed

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voltages V_r to the digital attenuator. The attenuator modifies V_r by N, producing a feedback voltage which is a function of itself, a fixed voltage, and the normalized output number.

Notes:

1. The error characteristics for this nonlinear digital system are superior to those of linear systems. Error expressed in percent of reading is more nearly constant and extension of scale length is possible.
2. The system produces attractive error profiles and can be implemented with only one component (a floating power supply or a summing amplifier) added to a conventional analog-to-digital converter.
3. Variation of the fixed voltage V, or the value of full scale, produces variations in the error profile.
4. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Ames Research Center
   Moffett Field
   Mountain View, California, 94035
   Reference: B65-10277

Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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